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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,580	11/16/2001	Salman Akram	MIO 0072 VA	9954

7590 04/23/2003

Killworth, Gottman, Hagan & Schaeff, L.L.P.
Suite 500
One Dayton Centre
Dayton, OH 45402-2023

EXAMINER	
MITCHELL, JAMES M	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,580	AKRAM, SALMAN	
	Examiner	Art Unit	
	James Mitchell	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20,23,24 and 52-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20,23,24 and 52-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 20, 53, 54 and 56 are rejected under 35 U.S.C. 102(e) as being anticipated by Ball (US 6,407,456).

Ball (Fig 2, 3) discloses:

a method of stacking a plurality of semiconductor die along a cross section, said method comprising: providing a substrate (18); inherently positioning, providing a first semiconductor die (14) adjacent said substrate, including a pair of major surfaces, wherein one of said pair of major surfaces of said first die defines a first active surface (opposite of 30) the other of said major surfaces of said first die defines a first stacking surface (30), and said first active surface includes at least one conductive bond pad (22); electrically coupling said first active surface to said substrate with at least one topographic contact (20) extending from a conductive bond pad on said first active surface to a conductive contact (26) on said substrate; inherently positioning, providing a second semiconductor die (64) adjacent said first die, including a pair of major surfaces, wherein one of said pair of major surfaces of said second die defines a

second active surface (56), the other of said major surfaces of said second die defines a second stacking surface, and said second active surface includes at least one conductive bond pad (58); and securing (28) said first stacking surface to said second stacking surface; wherein the first die is interposed between the substrate and the second die such that the second die defines an upper most die surface and the first die defines a lowermost die surface, and inherently positioning, securing an inherent decoupling capacitor (82) to said uppermost die surface of said second die and inherently conductively coupling said decoupling capacitor to at least one of said first and second dies; and interposing said second die between said capacitor and said first die; a conductive line (60) extending from a bond pad on said second active surface to a conductive contact on said first surface of said substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ball.

Ball is applied for the same reasons it was applied to claims 20, 53, 54 and 56. However, Ball does not appear to explicitly teach positioning a printed circuit board such that a first surface of said printed circuit board faces said substrate; and providing a plurality of topographic contacts extending from said second surface of said substrate to said first surface of said printed circuit board.

However examiner takes official notice that printed circuit boards were well known in the art at the time the invention was made and that it would have been obvious to one of ordinary skill in the art to form the stacked structure of Ball on a printed circuit board in order to mount the device in an electronic system.

Claims 23, 24 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee et al (US 20020074668) in combination with Spielberger et al (6,005,778).

Hofstee (Fig 1) discloses a method of assembling a printed circuit board, said method comprising: providing a substrate (not labeled) including fast and second surfaces and conductive contacts (not labeled) included on said first surface; providing a first semiconductor die (106) including a pair of major surfaces wherein one of said pair of major surfaces of said first die defines a first active surface (top portion), the other of said major surfaces of said first die defines a first stacking surface, said first active surface includes a plurality of conductive bond pads, and said first stacking surface is devoid of conductive bond pads; securing said first stacking surface to said first surface of said substrate between said conductive contacts included on said first surface of said substrate; providing a second semiconductor die (104) including a pair of major surfaces, wherein one of said pair of major surfaces of said second die defines a second active surface (lower portion), the other of said major surfaces (top) of said second die defines a second stacking surface, and said second active surface includes a plurality of inherent conductive bond pads (not labeled); electrically coupling said first semiconductor die to said second semiconductor die with a plurality of topographic contacts (108) extending from respective conductive, bond pads on said second

active surface to a corresponding conductive bond pad on said first active surface; positioning a printed circuit board (Par. 0008) such that a first surface of said printed circuit board faces said substrate; and providing a plurality of topographic contacts (116) extending from said second surface of said substrate to said first surface of said printed circuit board.

Hofstee does not appear to disclose securing a single decoupling capacitor to said second stacking surface; providing a pair of conductive lines, each of said conductive lines connecting a terminal of said decoupling capacitor, a bond pad on said first active surface, and a conductive contact on said first surface of said substrate; arranging said pair of conductive lines such that said decoupling capacitor is connected across Vss and Vcc pins of said first and second semiconductor dies.

Spielberger (Fig 5, 6) utilizes securing a single decoupling capacitor (70) to said second stacking surface; providing a pair of conductive lines (94), each of said conductive lines connecting a terminal of said decoupling capacitor, a bond pad on said first and second active surfaces, and a conductive contact on said first surface of said substrate; arranging said pair of conductive lines such that said decoupling capacitor is connected across Vss (72) and Vcc (74) pins of said first and second semiconductor dies

It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor to said second stacking surface in order to reduce propagation delays and transmission line effect as taught by Spielberger (Col. 1, Lines 38-39).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmm
April 18, 2003

DAVID E. GRAYBILL
PRIMARY EXAMINER